CISC 3320
C18d ARMv8 Architecture

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Acknowledgement

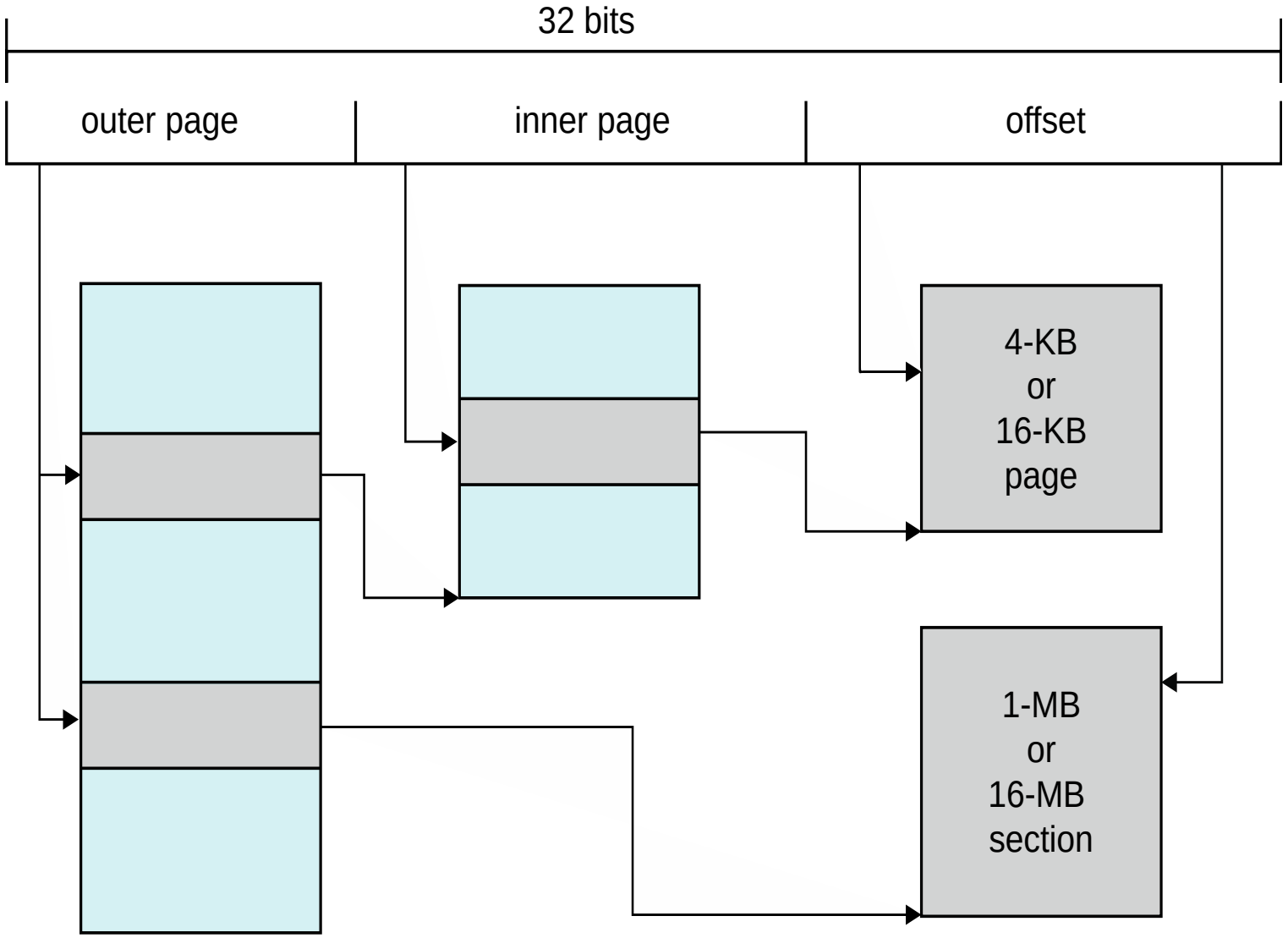
- These slides are a revision of the slides provided by the authors of the textbook via the publisher of the textbook

Outline

- Example: ARMv8 Architecture

Example: ARM Architecture

- Dominant mobile platform chip (Apple iOS and Google Android devices for example)
- Modern, energy efficient, 32-bit CPU
- 4 KB and 16 KB pages
- 1 MB and 16 MB pages (termed sections)
- One-level paging for sections, two-level for smaller pages
- Two levels of TLBs
  - Outer level has two micro TLBs (one data, one instruction)
  - Inner is single main TLB
  - First inner is checked, on miss outers are checked, and on miss page table walk performed by CPU


32 bits
outer page
inner page
offset
4-KB
or
16-KB
page
1-MB
or
16-MB
section

Questions?